



INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ :
HQ4M

 $\bar{A}2$

(11) International Publication Number: **WO 97/36411**

(43) International Publication Date: 2 October 1997 (02.10.97)

(21) International Application Number: PCT/US97/06085

(22) International Filing Date: 27 March 1997 (27.03.97)

(30) Priority Data: 08/625,398 27 March 1996 (27.03.96) US

(71) Applicant: HELLO DIRECT, INC. [US/US]; 5893 Rue Ferrari,
San Jose, CA 95138 (US).

(72) Inventor: STELMAN, Bruce, W.; 7448 Tulare Hills Drive, San Jose, CA 95139 (US).

(74) Agents: HAVERSTOCK, Thomas, B. et al.; Haverstock & Associates, Suite 420, 260 Sheridan Avenue, Palo Alto, CA 94306 (US).

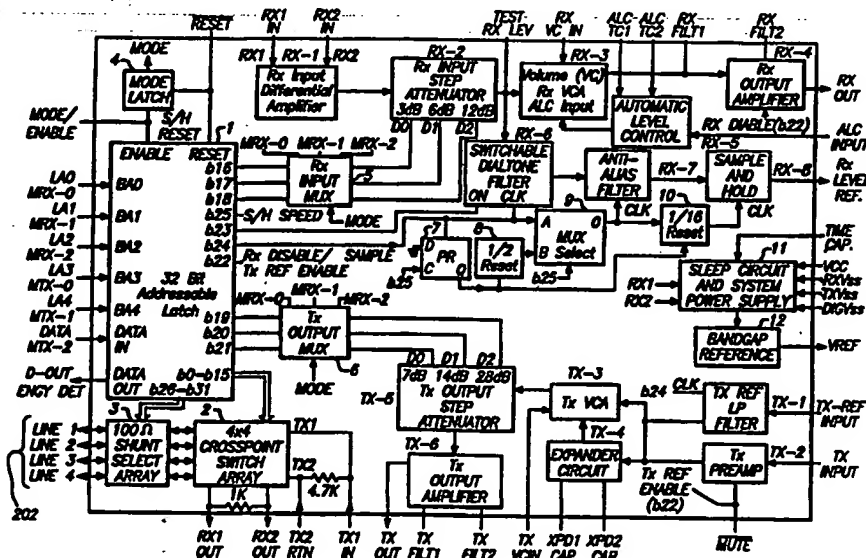
(81) Designated States: CA, CN, JP, KR, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published

Without international search report and to be republished upon receipt of that report.

RECEIVED
DEC 26 1997

(54) Title: SMART INTERFACE TECHNOLOGY



(57) Abstract

The present invention overcomes interface problems between proprietary handset ports on telephone base units and voice/data accessory products by allowing a user to automatically calibrate the telephone accessory product for an optimal interface match with the intended telephone base unit. This is accomplished through the use of a "Smart Interface Technology" (SIT) integrated chip set consisting of a full custom analog and semi-custom digital integrated circuit. The SIT incorporates three different methods for "learning" the characteristics of 4-wire port modular interfaces found in all telephone station sets. Basically, these methods determine the appropriate 4-wire terminal configurations, the transmit and receive channels of the intended telephone base unit, and adjust the channel sensitivities until an optimal and clear signal is provided for the user.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav Republic of Macedonia	TM	Turkmenistan
BF	Burkina Faso	GR	Greece			TR	Turkey
BG	Bulgaria	HU	Hungary	ML	Mali	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MN	Mongolia	UA	Ukraine
BR	Brazil	IL	Israel	MR	Mauritania	UG	Uganda
BY	Belarus	IS	Iceland	MW	Malawi	US	United States of America
CA	Canada	IT	Italy	MX	Mexico	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NE	Niger	VN	Viet Nam
CG	Congo	KE	Kenya	NL	Netherlands	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NO	Norway	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's Republic of Korea	NZ	New Zealand		
CM	Cameroon	KR	Republic of Korea	PL	Poland		
CN	China	KZ	Republic of Korea	PT	Portugal		
CU	Cuba	LC	Kazakhstan	RO	Romania		
CZ	Czech Republic	LI	Saint Lucia	RU	Russian Federation		
DE	Germany	LK	Liechtenstein	SD	Sudan		
DK	Denmark	LR	Sri Lanka	SE	Sweden		
EE	Estonia		Liberia	SG	Singapore		

Smart Interface Technology

Field of the Invention

This invention relates to the field of telephony. More particularly, this invention relates to a device capable of providing a 4-wire interface to any
5 telephone base unit's handset/headset port using 2-wire each send and receive lines.

Background of the Invention

For purposes of this discussion, a telephone network can be considered as being divided into two parts. The first part comprises everything from the telephone company leading up to and including the Central Office (CO) termination
10 point in a subscriber's home or office. The second part comprises everything from the Central Office termination point and includes the individual telephone sets connected directly to this termination point as well as proprietary systems (Key/PBX) and their respective proprietary telephone sets.

Everything within the first part is regulated by the Federal Communications
15 Commission (FCC) and therefore has a standard to which telephone set and system manufacturers must base their interface equipment. This includes all devices connecting directly to the Central Office telephone network, including telephone sets and telephone systems. One problem that the telephony industry faces is that the other parts of the telephone network are not regulated, including anything
20 related to the telephone sets which is not connected directly to the telephone network, such as proprietary telephone sets and all hand sets.

Private phones generally include a telephone base unit and modular accessories, such as a handset/headset. Accordingly, telephone manufacturers can and do develop independent interface systems between their telephone base units
25 and accessories such as handsets/headsets. This often precludes the use of a different type of handset/headset with a particular base unit without manual reprogramming. The problem is especially apparent when dealing with Key and Private Branch Exchange (PBX) system station sets which are entirely proprietary

in nature. Many manufacturers are providing accessories which are provided as original equipment with the base unit. Many of these accessory products provide both voice and data solutions not offered in the telephone station sets such as headset, teleconferencing, facsimile and modem communication alternatives.

5 What is needed is an invention that will allow a user to automatically calibrate a commercially available non-regulated voice/data product to allow an effective interface. This would solve any incompatibility problems and provide users with greater choices and flexibility when selecting telephone equipment.

Summary of the Invention

10 The present invention overcomes interface problems between proprietary handset ports on telephone base units and voice/data accessory products by allowing a user to automatically calibrate the telephone accessory product for an optimal interface match with the intended telephone base unit. This is accomplished through the use of a "Smart Interface Technology" (SIT) integrated
15 chip set consisting of a full custom analog and semi-custom digital integrated circuit. The SIT incorporates three different methods for "learning" the characteristics of 4-wire port modular interfaces found in most telephone station
20 sets. These methods determine the appropriate 4-wire terminal configurations, the transmit and receive channels of the intended telephone base unit, and adjust the channel sensitivities until an optimal and clear signal is provided for the user.

Brief Description of the Drawings

Figure 1 illustrates a flow model of a "Central Office (CO) Dialtone Learning Sequence."

5 Figure 2 illustrates a flow model of the "Automated 800 Learning Sequence."

Figure 3 illustrates a diagram of the SIT Data Transmission technique used for the "Automated 800" and "Manual 800" Learning Sequences of the present invention.

Figure 4 illustrates switching algorithms for the system.

10 Figure 5 is a continuation of the switching algorithms of Figure 4.

Figure 6 illustrates a block diagram of the regulated and non-regulated portions of a typical telephone interface configuration as it relates to both the Central Office and the "Smart Interface Technology" (SIT) system connection of the present invention.

15 Figure 7 illustrates a block diagram of the SIT system including a full-custom analog and semi-custom digital microcontroller integrated circuit.

Figure 8 illustrates a block diagram of the SIT full-custom analog integrated circuit of the present invention.

20 Figure 9 illustrates a block diagram of 4x4 crosspoint switch and shunt resistor arrays.

Detailed Description of the Preferred Embodiment

Figure 1 is a flow model of the "CO Dialtone Learning Sequence." This is the primary method the SIT system uses to "learn" the characteristics of the telephone interface. The "CO Dialtone Learning Sequence" is automatic and
25 transparent to the end user.

Upon initial system power-up, such as the first time batteries are installed, a "CO Dialtone Search" routine is enabled to detect and locate a CO dialtone signal on any combination of the 4-wire interface lines from the telephone base unit.

When the CO dialtone is detected, the "CO Dialtone Learning Sequence" will be fully enabled.

The "CO Dialtone Learning Sequence" is a one time activation process. After a successful "learn sequence" has been executed, the appropriate bit
5 addressable latch 1 settings are stored from the digital MCU 100 into the EEPROM 300, in order to maintain the correct settings in the event of a power failure. Subsequent CO dialtones will not enable the learning sequence unless a system reset is performed to re-enable the learning routine. The "CO Dialtone Learning Sequence" is re-enabled by a user depressing the system reset switch 258 for a
10 minimum of five seconds or by a soft system reset which is accessed remotely.

The "CO Dialtone Learning Sequence" starts with the location of the CO dialtone. Location of the CO dialtone indicates the proper receive lines. The receive input step attenuator then adjusts the receive channel sensitivity based on reference levels as described above. The transmit lines are then selected and the
15 transmit output step attenuator adjusts the transmit channel sensitivity based on reference levels.

Figure 2 illustrates the flow models of the SIT "Automated 800 Learning Sequence." Due to the lack of regulation as it relates to Key and PBX system
station sets, there is a wide variation of sidetone characteristics which may be
20 encountered. Consequently, it is possible that occasionally, the learning method employed by the "CO Dialtone Method" may not provide optimal overall SIT system performance. The "Automated 800 Method" provides a very accurate means for the SIT system to "learn" the characteristics of a 4-wire telephone port interface.

25 The "Automated 800 Learning Method" involves interaction between a "Host" system located at the termination of the accessed telephone line and the "SIT" system located at the end user's location. The user places a call to a designated telephone number and is greeted by an "automated attendant" message. In the case of a voice application such as a headset interface, the message instructs
30 the user to momentarily depress the system reset switch 258, place the

"handset/headset" switch to the "headset" position and press a key on the telephone set keypad. The keystroke interrupts the "auto attendant" message and the "Host" sends a preamble to the "SIT" system. When the preamble is detected, the "Automated 800 Learning Method" is enabled.

5 The "Automated 800 Learning Method" interaction between the "Host" and "SIT" systems is shown in the flow model illustrated in Figure 2 and the "FSK Data Transmission Diagram" is illustrated in Figure 3. The "Host" sends a preamble, for a predetermined amount of time, to the "SIT" system to initiate the "Automated 800 Learning Sequence." The "Host" then sends a 1 KHz reference
10 signal, for a predetermined amount of time, for setup/calibration of the "SIT" system which it compares to an internal reference and uses to ensure proper setup/calibration of the "SIT" system transmit channel. When the incoming 1 KHz reference level is satisfied, the "Host" sends a level confirmation signal to the "SIT" system and a final "handshake" is generated between the "Host" and "SIT"
15 systems signifying completion of the "Automated 800 Learning Sequence."

 The SIT "Automated 800 Learning Sequence" begins by searching for the preamble sent by the Host. Once the preamble is located, the proper receive lines are located. The receive channel sensitivity is then adjusted in comparison to a receive level reference. Upon locating the proper receive lines, the transmit lines
20 are selected and their sensitivity is adjusted in comparison to a transmit level reference signal.

 A third and final interface method is the "Manual 800 Method." This method is used when either of the previously described learning sequences fail to provide optimal performance with a particular telephone port interface. The
25 "Manual 800 Method" provides the user with the ability to interact with a trained telephony technician whom has the ability to adjust virtually all of the SIT parameters remotely with the use of a second "Host" system.

 The SIT system "CO Dialtone" and "Automated 800 Learning" methods will select the most common configurations which satisfy the system's performance
30 criteria. Occasionally this may not be the optimal "line configuration" selection for

all interface environments. Since there are no regulatory requirements governing the specific characteristics for 4-wire handset port interfaces, there is a range of different configurations. It is not uncommon for an electronic telephone set to contain a handset port interface that will operate with multiple "line-configuration" settings. All of the configurations will provide acceptable system performance, occasionally however, a particular configuration will be more susceptible to unwanted radio-frequency interference or electro-magnetic interference. In these cases, alternate combinations must be selected for optimal system performance.

Alternate combinations can be implemented by a user placing a call to a technical support staff member (tech) at a designated telephone number. After determining the problematic symptoms, the technician has the ability to enable the "CO Dialtone Learning Sequence," the "Automated 800 Learning Sequence" or the "Manual 800 Method" modes of operation by sending the appropriate sequence preamble. In the "Manual 800 Method" mode of operation, the technician can directly manipulate and change the parameters associated with the crosspoint switch array 2, the receive input step attenuator RX-2 or the transmit output step attenuator TX-5.

A block diagram of the regulated and non-regulated portions of a typical telephone interface configuration is illustrated in Figure 6. The connection between the Central Office Lines of the telephone company 52 and either a telephone set 54 or a telephone system 56 is regulated. Accordingly, telephone sets and systems from many manufacturers can all be connected directly to the Central Office lines 52. The connection between a telephone system 56 and a hybrid or digital telephone set 58 is not regulated. The connection between a telephone set 54 or 58 and an accessory 60 or 62 is also not regulated. Therefore, unless designed to interface, one manufacturer's accessory may not operate with another manufacturer's telephone set.

The present invention provides a "Smart Interface Technology" (SIT) system interface 50 which provides an interface between accessories 60 and 62 and telephone base units 54 and 58, having different protocols. The SIT system

interface 50 allows a voice/data accessory 60 or 62 to be used with telephone base units 54 and 58 from multiple manufacturers, each having different protocols.

A block diagram of the SIT interface system of the present invention is illustrated in Figure 7. The preferred embodiment of the SIT interface system includes a full-custom SIT analog integrated circuit 200, a semi-custom digital microcontroller (MCU) 100, a 1-K serial EEPROM 300, a 4-wire telephone handset port 202 for coupling to a base unit, a voice or data 2-channel interface input port 204 and output port 206.

The analog integrated circuit 200 is coupled to the telephone handset port 202 through a 4-wire line interface. This interface allows for the establishment and selection of the 2-wire each send (Tx) and receive (Rx) line pairs. As is well known, the send and receive pairs are frequently not the same two lines in the port and may often share a common return signal line.

Outputs P4 through P10 of the Digital MCU 100 are coupled to inputs LA0 through LA4, DATA IN and MODE/ENABLE of the analog integrated circuit 200, respectively. It is through this coupling that the digital MCU 100 is able to control the various blocks within the analog integrated circuit 200, which will be discussed below.

A receive signal Rx REF OUT of the analog integrated circuit 200 is coupled to the analog/digital (A/D) input of the digital MCU 100 and provides a sample of the input signal which the analog integrated circuit 200 receives from the telephone base unit. The digital MCU 100 uses this information to determine if the appropriate line configuration has been selected and to control the receive and transmit channel sensitivities.

A signal TONE OUT from the digital MCU 100 is coupled to an input TXREF of the analog integrated circuit 200 and allows the digital MCU 100 to provide a 1 KHz. calibration transmit tone, through the analog integrated circuit 200, to facilitate the appropriate selections of the transmit lines and transmit channel sensitivity setting.

An input RESET of both the Digital MCU 100 and analog integrated circuit 200 is coupled to a power-on reset circuit and switch 250. The reset input 250 allows the SIT system to be reset to activate one of the three "learning sequences" for the SIT system, of the present invention, to "learn" the characteristics of the telephone base unit. The reset circuit 250 is coupled to a reset switch 258 which is activated by a user.

A serial 1K EEPROM 300 is coupled to the digital MCU 100 and stores the "learned" characteristics of the attached telephone base unit after a successful "learning sequence" has been executed. The "learned" settings for controlling the analog integrated circuit 200 are thereby maintained within the EEPROM 300 in the event of a power failure.

A crystal oscillator 208 is coupled to inputs Xin and Xout of the digital MCU 100 for generation of a clock signal by the digital MCU 100 which controls the overall system timing of the SIT system interface 50 of the present invention.

The receive volume control 252 is coupled to an input RX VC IN of the analog integrated circuit 200 and is primarily used in voice applications whereby the user can adjust an output level of the received signal to achieve a comfortable listening level.

The transmit volume control 254 is coupled to an input TX VC IN of the analog integrated circuit 200 and is used as a fine tuning adjustment for precise level matching of the transmitted signal with the telephone base unit.

The mute switch 256 is coupled to an input MUTE of the analog integrated circuit 200 and is primarily used in voice applications whereby the user can disable the transmit preamplifier to temporarily prevent any signals from being transmitted to the telephone base unit.

The transmit channel voice or data input port 204 is coupled to an input MIC IN on the analog integrated circuit 200. This is the primary input point between the user and the SIT system of the present invention. In voice applications, the input MIC IN is preferably coupled to an electret type microphone.

The receive channel voice or data output port 206 is capacitively coupled from an output RX OUT of the analog integrated circuit 200 and provides the equalized incoming signal from the telephone base unit to the user. In voice applications, the output RX OUT is preferably coupled to an audio loudspeaker.

5 The output RX OUT is also coupled to an input ALC IN of the analog integrated circuit 200 which acts as a compressor for large unwanted signals which are potentially harmful to the user or interface apparatus.

The digital MCU 100, analog integrated circuit 200 and serial 1K EEPROM 300 are preferably battery powered and can operate over a supply range of 3 to 5
10 volts DC. The digital MCU 100 is coupled to the bandgap DC reference voltage generated by the analog integrated circuit 200.

Timing capacitors 210, 212, 214 and 216 are coupled to inputs XPND1, XPND2, ALC TC2 and ALC TC1, of the analog integrated circuit 200, respectively. These timing capacitors 210, 212, 214 and 216 are then coupled to
15 various blocks within the analog integrated circuit 200 and used to control the various attack and release times associated with expander, compressor and sleep circuits.

Filter capacitors 218, 220, 222 and 224 are coupled to inputs TX FILT1, TX FILT2, RX FILT1 and RX FILT2 of the analog integrated circuit 200,
20 respectively. These filter capacitors 218, 220, 222 and 224 are then coupled to the receive and transmit channel output amplifiers and are used to set the channel frequency response characteristics.

Coupling capacitor 226 is coupled between a receive input RX1 IN and a receive output RX1 OUT of the analog integrated circuit 200. Coupling capacitor
25 228 is coupled between a receive input RX2 IN and a receive output RX2 OUT of the analog integrated circuit 200. Coupling capacitor 230 is coupled between a transmit input TX1 IN and a transmit output TX OUT of the analog integrated circuit 200. Coupling capacitor 232 is coupled between an input TX2 RET of the analog integrated circuit 200 and ground. Coupling capacitor 234 is coupled
30 between the input MIC IN of the analog integrated circuit 200 and the voice/data

input port 204. Coupling capacitor 236 is coupled between an output RX OUT of the analog integrated circuit 200 and the voice/data output port 206. The coupling capacitors 226, 228, 230, 232, 234 and 236 are used to remove DC offset and couple the AC input and output signals into and out of the various send and receive signal blocks found in both the receive and transmit channels of the analog integrated circuit 200.

A system block diagram of the preferred embodiment of the SIT analog integrated circuit 200 is illustrated in Figure 8. The SIT analog integrated circuit 200 is a full custom circuit that is designed to interface directly to the telephone base unit and is controlled by the semi-custom digital MCU 100, as illustrated in Figure 7.

Within the analog integrated circuit 200, a 32 bit addressable latch 1 includes inputs BA0-BA4 which are coupled to the pins LA0-LA4 of the analog integrated circuit 200. An input DATA IN and output DATA OUT of the 32 bit addressable latch 1 are coupled to the pins DATA IN and DATA OUT, respectively, of the analog integrated circuit 200. An enable input ENABLE of the latch 1 is coupled to a mode latch 4 and to the pin ENABLE of the circuit 200. A reset input RESET of the latch 1 is coupled to the mode latch 4 and to the pin RESET of the circuit 200. The mode latch 4 is controlled by the signals from the pins ENABLE and RESET and saves a current mode which the circuit 200 is operating in. Outputs b0-b15 of the latch 1 are coupled to control a 4x4 crosspoint switch array 2. Outputs b16-b18 of the latch 1 are coupled to control a receive input multiplexer 5. Outputs b19-b21 of the latch 1 are coupled to control a transmit output multiplexer 6. Output b22 of the latch 1 provides a receive/transmit disable/enable control signal. Output b23 of the latch 1 is coupled to an input ON of a switchable dialtone filter RX-6. Output b24 of the latch 1 is coupled to an input PR of a flip-flop 7, to an input A of a multiplexer 9 and to a clock input CLK of the switchable dialtone filter RX-6. Output b25 of the latch 1 provides a signal S/H SPEED which is coupled to an input C of a flip-flop 7 and

to a select input of the multiplexer 9. Outputs b26-b31 of the latch 1 are coupled to control a 100 ohm shunt select array 3.

5 The four lines of the 4-wire phone port 202 are coupled as inputs to the array 3. The array 3 is also coupled to the array 2. Outputs of the array 2 are coupled to the pins RX1 OUT and RX2 OUT of the analog integrated circuit 200 to provide an output received signal. Inputs of the array 2 are coupled to the pins TX1 IN and TX2 RTN of the circuit 200, to receive a transmit signal. Outputs of the multiplexer 5 are coupled as inputs D0, D1 and D2 of a receive input step attenuator RX-2. Two sets of control inputs MRX-1, 2, 3, and BITS 16, 17, 18 are
10 coupled to multiplexer 5. Outputs of multiplexer 6 are coupled as inputs D0, D1 and D2 of a transmit output step attenuator TX-5. Two sets of control inputs MTX-1, 2, 3 and BITS 19, 20, 21 are coupled to multiplexer 6. An output MODE of the mode latch 4 is coupled to the selection control inputs of multiplexers 5 and 6.

15 The receive input pins RX1 IN and RX2 IN of the analog integrated circuit 200 are coupled as inputs to a receive input differential amplifier RX-1. An output of the amplifier RX-1 is coupled as an input to the receive input step attenuator RX-2. An output of the attenuator RX-2 is coupled as an input to a receive voltage controlled amplifier (VCA) RX-3, as an input to a switchable dialtone filter RX-6
20 and to a pin TEST RX LEV of the circuit 200 for testing the level of the received signal output from the attenuator RX-2.

A receive voltage control pin RX VC IN of the circuit 200 is coupled as a control input to the receive VCA RX-3. Automatic level control (ALC) pins ALC TC1, ALC TC2 and ALC INPUT of the circuit 200 are coupled as inputs to an
25 ALC circuit RX-5. An output of the ALC circuit RX-5 is coupled as an ALC input to the receive VCA RX-3. An input of the receive VCA RX-3 is coupled to a receive filter pin RX FILT1 of the circuit 200 and as an input to a receive output amplifier RX-4. An output b22 of the latch 1 is coupled as a receive disable input to the amplifier RX-4. An output of the amplifier RX-4 is coupled to a receive
30 filter pin RX FILT2 of the circuit 200. A receive output signal is provided as an

output from the amplifier RX-4 and coupled to a receive output pin RX OUT of the circuit 200.

5 A transmit reference input pin TX REF INPUT of the circuit 200 is coupled as an input to a transmit reference filter TX-1. An output b24 of the latch 1 is coupled as a clock input to the filter TX-1. A transmit input pin TX-INPUT of the circuit 200 is coupled as an input to a transmit pre-amplifier circuit TX-2. A mute pin MUTE of the circuit 200 is coupled as an input to the pre-amplifier circuit TX-2. The output b22 of the latch 1 is coupled as transmit enable input to the pre-amplifier circuit TX-2. An output of the pre-amplifier circuit TX-2 is coupled to an output of the filter TX-1 and as an input to a transmit VCA TX-3 and an expander circuit TX-4.

10 Pins XPD1 CAP and XPD2 CAP of the circuit 200 are coupled as inputs to the expander circuit TX-4. An output of the expander circuit TX-4 is coupled as an input to the transmit VCA TX-3. A transmit pin TX VCIN of the circuit 200 is coupled to an input of the transmit VCA TX-3. An output of the transmit VCA TX-3 is coupled as an input to the transmit output step attenuator TX-5. An output of the attenuator TX-5 is coupled as an input to a transmit output amplifier TX-6. Transmit filter pins TX FILT1 and TX FILT2 of the circuit 200 are coupled to inputs of the amplifier TX-6. A transmit output signal is output from the amplifier TX-6 and coupled to the transmit output pin TX OUT of the circuit 200.

20 An input D of the flip-flop 7 is coupled to ground. An output Q of the flip-flop 7 is coupled as a reset input to a 1/2 dividing circuit 8 and a 1/16 dividing circuit 10. An output of the 1/2 dividing circuit 8 is coupled as an input B to the multiplexer 9. An output O of the multiplexer 9 is coupled as an input to the 1/16 dividing circuit 10 and to an anti-alias filter circuit RX-7. An output of the switchable dialtone filter circuit RX-6 is coupled as an input to the filter RX-7. An output of the filter RX-7 is coupled as an input to a sample and hold circuit RX-8. An output of the 1/16 dividing circuit 10 is coupled as an input to the sample and hold circuit RX-8. An output of the sample and hold circuit RX-8 is coupled to a receive level reference pin RX LEVEL REF of the circuit 200.

25

30

A timing capacitor pin TIME CAP of the circuit 200 is coupled as an input to a sleep circuit and system power supply 11. Power supply input pins VCC, RXVss, TXVss and DIGVss of the circuit 200 are coupled as inputs to the sleep circuit and system power supply 11. The inputs RX1 and RX2 to the amplifier RX-1 are coupled as inputs to the sleep circuit and system power supply 11. An output of the sleep circuit and system power supply 11 is coupled to a bandgap reference circuit 12. An output of the bandgap reference circuit 12 is coupled to a voltage reference pin VREF of the circuit 200.

The digital MCU 100 is able to address and manipulate the 32 bit addressable latch 1, thereby controlling the 4x4 crosspoint switch array 2 and 100 ohm resistor shunt array 3, within the analog integrated circuit 200. The crosspoint switch array 2 has four input ports which are directly coupled to a four line telephone base unit jack 202 through the array 3, as illustrated by the lines 1-4. The 100 ohm resistor shunt array 3 contains six switchable shunt resistors, is configured in parallel with the crosspoint switch array 2 input ports, and is capable of providing a 100 ohm shunt resistance between any of the 4 line inputs.

When a telephone accessory including the interface system of the present invention is first plugged into a telephone base unit, the accessory may not operate because it has not yet been optimally configured to electronically communicate with the telephone base unit. A Central Office dialtone is applied by the telephone base unit to two of the lines of the jack 202. Under control of the digital MCU 100, the addressable latch 1 manipulates the crosspoint array 2 and the shunt select array 3 by sequentially coupling pairs of line input ports until a CO dialtone is sensed by the digital MCU 100 in the receive channel. This information is then latched for further analysis by the digital MCU 100.

The two receive lines through which a CO dialtone is detected, are coupled to the receive input differential amplifier RX-1 which is terminated with a known resistive impedance. In the preferred embodiment, the resistive impedance is 1K ohm.

A 28 dB energy variance exists between telephones that are commercially available. Accordingly, in a voice application, a telephone headset or other accessory that is configured to work with one telephone base unit could provide an uncomfortably loud signal when used with a second base unit or be significantly quiet when used with a third telephone base unit. To solve this problem, the output of the differential amplifier RX-1 is coupled to the input of the receive step attenuator RX-2. The receive step attenuator RX-2 is initially configured to provide maximum attenuation and then increases the receive signal in 4 dB increments until a predetermined target reference level is sensed by the digital MCU 100, thereby equalizing the receive channel sensitivity. The receive step attenuator RX-2 is coupled to the receive input multiplexer 5 which is controlled by the 32 bit addressable latch 1. The digital MCU 100 controls both the bit addressable latch 1 and the receive input multiplexer 5 thereby setting the attenuation by the step attenuator RX-2.

The equalized receive signal is then coupled to the voltage controlled amplifier RX-3 which can have fixed gain or allow the user to manually control the volume level of the receive signal through a port RX VC IN which is coupled to the voltage controlled amplifier RX-3. An output of the automatic level control circuit RX-5 is also coupled to an ALC control input on the voltage controlled amplifier RX-3 and is capable of controlling the amplifier gain.

The automatic level control circuit RX-5 acts as a dynamic output limiting system with an overall dynamic range of 40 dB. The automatic level control circuit RX-5 input samples the output level of the receive channel and has a selectable limiting threshold as shown in Figure 7 which is adjusted using the ALC level adjust circuit 260. The automatic level control circuit RX-5 is capable of limiting the output level of the receive signal to a predetermined level to prevent large unwanted and potentially harmful signals from reaching a user. In voice applications, the user's ears will be protected from prolonged high decibel sounds by the automatic level control circuit RX-5, thereby preventing potential damage to the user's hearing. The ALC timing capacitors 214 and 216, illustrated in Figure

7, are coupled to the pins ALC TC1 and ALC TC2 and are used to set the attack and release timing characteristics of the ALC circuit RX-5.

The equalized receive signal is output from the receive VCA RX-3 and coupled as an input to the receive output amplifier RX-4 which is capable of driving resistive, capacitive and inductive loads via the receive output-port RX OUT for compatibility with voice or data interfaces. The filtering capacitors 222 and 224, illustrated in Figure 6, and coupled to the pins RX FILT1 and RX FILT2 of the circuit 200 are used to determine the receive channel frequency response.

The digital MCU 100 monitors the receive signal by sampling the signal through the receive level reference port RX LEVEL REF. The receive signal sample for the digital MCU 100 is taken at the output of the receive step attenuator RX-2 and is filtered by the dialtone filter RX-6, then the anti-alias filter RX-7. The receive signal sample is finally coupled into the sample and hold circuit RX-8 prior to being passed on to the receive level reference port RX LEVEL REF. The receive level reference port RX LEVEL REF is coupled directly to the A/D input of the digital MCU 100. The digital MCU 100 controls the dialtone filter RX-6, anti-alias filter RX-7 and sample and hold circuit RX-8 via the 32 bit addressable latch 1 and synchronizes these switched capacitor filters with the use of the clock circuitry shown in the blocks 7, 8, 9 and 10.

Once the receive lines are determined and the channel sensitivity is adjusted for optimal performance, the transmit lines and sensitivity are then determined. Based on the selected receive lines, certain transmit line configurations are highly probable and are prioritized in the system algorithms.

Utilizing the sidetone characteristics of telephone base units, the digital MCU 100 will continue to monitor the receive signal path via the receive level reference output port RX LEVEL REF for calibration of the transmit channel.

A transmit preamplifier TX-2 is used as the interface for the user voice or data input signal and provides some preamplification of the input signal in addition to a channel mute user portion. It should be noted that this mute stage is disabled during the "learning" process to prevent the user from inserting a variant signal into

the transmit path. The output of the transmit preamplifier TX-2 is coupled to the transmit VCA TX-3 and the transmit expander circuit TX-4.

During a "learning" procedure, the digital MCU 100 generates a 1KHz transmit calibration signal into the transmit reference input port TX REF INPUT. The 1 KHz calibration signal is then coupled into the transmit reference low pass filter TX-1 which is controlled by the 32 bit addressable latch 1 and hence the digital MCU 100. The transmit reference low pass filter TX-1 filters out the odd harmonics of the calibration signal and outputs the result to the transmit VCA TX-3 and the expander circuit TX-4.

The input of the expander circuit TX-4 is coupled to the output of the transmit preamplifier TX-2 and the transmit reference low pass filter TX-1. The expander circuit TX-4 differentiates input noise from the desired signal. The expander circuit TX-4 output is coupled to a control input of the transmit VCA TX-3 and provides electronic noise reduction by attenuating the transmit VCA gain as it relates to unwanted background noise. The timing capacitors 210 and 212, illustrated in Figure 7 and coupled to the pins XPD1 and XPD2 are used to determine the expander attack and release characteristics.

The transmit VCA TX-3 receives its input from the transmit preamplifier TX-2 and transmit reference low pass filter TX-1 and serves two primary purposes.

The transmit VCA TX-3 works in conjunction with the transmit expander circuit TX-4 to provide electronic noise reduction and provides an overall transmit channel output level adjustment to allow precise interface matching via an optional transmit volume control function. The transmit volume control circuit 254 is illustrated in Figure 7. The output of the transmit VCA TX-3 is coupled to the transmit output step attenuator TX-5.

The digital MCU 100 will begin manipulating the crosspoint switch array 2 by sequentially coupling pairs of the transmit output ports starting with the most probable pairs defined in the system algorithms. A description, which illustrates the system's switching algorithms, is shown in detail in Figures 4 and 5. The 1 KHz transmit calibration signal is therefore applied to the telephone base unit via

the jack lines 202 until the 1 KHz signal is sensed by the digital MCU 100 at the receive level reference output RX LEVEL REF. When the digital MCU 100 senses the 1 KHz signal it will have successfully located the appropriate transmit lines and will latch the information and begin the transmit output step attenuator TX-5
5 adjustment.

A 49 dB variance in transmit line sensitivity exists between telephone base units that are commercially available. A precise sensitivity interface match is critical for optimal performance of the transmitted signal with the various telephone base units. To solve this problem, the signal output of the transmit VCA TX-3 is
10 coupled into the transmit output step attenuator TX-5 which effects the transmit output level. The transmit output step attenuator TX-5 is coupled to the transmit output multiplexer 6 which is controlled by the 32 bit addressable latch 1 and therefore the digital MCU 100. The digital MCU 100 will adjust the transmit step attenuator in 7 dB increments until a predetermined 1 KHz target reference level is
15 sensed by the digital MCU 100, thereby equalizing the transmit channel sensitivity to the appropriate level. The signal output of the transmit output step attenuator TX-5 is coupled to the transmit output amplifier TX-6.

The transmit output amplifier TX-6 is capable of providing a voltage or current drive output and driving resistive, capacitive or inductive loads. A coupling
20 capacitor 230 is used to couple the transmit output signal from the pin TX OUT into the crosspoint switch array 2 through the transmit input pin TX1 IN. The filtering capacitors 218 and 220, illustrated in Figure 7 and coupled to the pins TX FILT1 and TX FILT2 are used to determine the transmit channel frequency response.

To conserve on battery life of the power supply 11, the analog integrated circuit 200 includes the sleep circuit within the power supply 11. The sleep circuit
25 11 is coupled between the VCC port and the main IC block power supplies. The sleep circuit control input is coupled to the inputs RX1 and RX2 of the receive differential amplifier RX-1. If the incoming broadband noise on the receive lines
30 drops below a certain level, preferably -65 dBV, the sleep circuit begins a timing

sequence as determined by the value of the sleep timing capacitor 218. If the broadband receive signal does not exceed the -65 dBV threshold within the programmed timeframe, the analog integrated circuit 200 enters into the sleep mode and shuts down. When the broadband receive signal exceeds the -65dBV
5 threshold, the sleep timing sequence resets and the analog integrated circuit "wakes up" within 5 milliseconds (ms).

The preferred embodiment for the analog integrated circuit 200 is powered by any convenient power source which can be directly connected to the pin VCC to serve as the primary circuit power supply. The bandgap reference circuit 12
10 develops a stable reference voltage for use internally in the analog integrated circuit 200 and externally for the digital MCU 100 and VCA control voltages.

A block diagram of the 4x4 crosspoint switch array 2 and the 100 ohm shunt resistor array 3 is illustrated in Figure 9. The crosspoint switch array consists of a 4x4 matrix of analog switches designed to connect lines 1-4 of the 4-
15 wire phone port 202 to the two transmit and two receive channels in any order and polarity. It is under the control of the digital MCU 100, through the bit addressable latch 1, that the appropriate transmit and receive lines are determined, as described above.

The present invention has been described in terms of specific embodiments
20 incorporating details to facilitate the understanding of the principles of construction and operation of the invention. Such reference herein to specific embodiments and details thereof is not intended to limit the scope of the claims appended hereto. It will be apparent to those skilled in the art that modifications may be made in the embodiment chosen for illustration without departing from the spirit and scope of
25 the invention. Specifically, it will be apparent to one of ordinary skill in the art that the method of the present invention could be implemented in several different ways and the apparatus disclosed above is only illustrative of the preferred embodiment of the present invention and is in no way a limitation.

C L A I M S

We claim:

1. A telecommunications interface system that automatically configures an accessory having a predetermined number of electrical accessory contacts to appropriately interface with a telephone base unit having two electrical output contacts, wherein the interface system is configured for coupling the output contacts to a predetermined pair of the accessory contacts, the interface comprising:

- a. an interface port having the predetermined number of accessory contacts, wherein the port receives an input signal from the output contacts on two of the accessory contacts;
- b. a signal processing circuit having two signal inputs coupled for receiving the input signal from the interface port; and
- c. a directing circuit coupled between the interface port and the signal processing circuit for automatically electrically coupling the output contacts to the signal inputs.

2. The telecommunications interface system according to claim 1 wherein the base unit further comprises two electrical input contacts, wherein the interface system is configured for coupling the input contacts to a predetermined pair of the accessory contacts,

- a. the signal processing circuit further comprising two signal outputs coupled for providing an output signal;
- b. the interface port further comprising means for receiving the output signal from the signal outputs on two of the accessory contacts; and
- c. the directing circuit further comprising means for electrically coupling the signal outputs to the input contacts.

1 3. The telecommunications interface system according to claim 2 wherein the
2 signal processing circuit further comprises means for controlling the directing
3 circuit in order to manipulate the coupling of the input and output contacts with the
4 signal inputs and outputs.

1 4. The telecommunications interface system according to claim 3 wherein the
2 interface system further comprises a decisional circuit coupled to the means for
3 controlling the directing circuit, in order to configure the means for controlling the
4 directing circuit.

1 5. The telecommunications interface system according to claim 4 wherein the
2 signal processing circuit further comprises a differential amplifier coupled to the
3 directing circuit for receiving the input signal from the base unit, regardless of
4 polarity.

1 6. The telecommunications interface system according to claim 5 wherein the
2 analog circuit further comprises an output automatic gain adjusting circuit coupled
3 to the differential amplifier for providing an adjusted input signal having a
4 predetermined range of amplitudes.

1 7. The telecommunications interface system according to claim 6 further
2 comprising a reference signal, wherein the output automatic gain adjusting circuit
3 adjusts the input signal to a predetermined reference signal level.

1 8. The telecommunications interface system according to claim 6 wherein the
2 signal processing circuit further comprises means for manually controlling the
3 output automatic gain adjusting circuit coupled between the output automatic gain
4 adjusting circuit and the addressable latch.

1 9. The telecommunications interface system according to claim 7 wherein the
2 signal processing circuit further comprises means for controlling the volume of the
3 input signal coupled between the automatic gain adjusting circuit and the
4 addressable latch.

1 10. The telecommunications interface system according to claim 9 wherein the
2 signal processing circuit further comprises an automatic level control circuit
3 coupled to the means for controlling the volume, for providing a dynamic output
4 limiting system.

1 11. The telecommunications interface system according to claim 9 wherein the
2 signal processing circuit further comprises an output amplifier coupled to the
3 volume control amplifier for driving an inductive load.

1 12. The telecommunications interface system according to claim 11 wherein the
2 inductive load is a headset.

1 13. The telecommunications interface system according to claim 11 wherein the
2 inductive load is a handset.

1 14. The telecommunications interface system according to claim 9 wherein the
2 signal processing circuit further comprises means for sampling the input signal
3 coupled between the automatic gain adjusting circuit and the means for controlling
4 the directing circuit.

1 15. The telecommunications interface system according to claim 4 wherein the
2 signal processing circuit further comprises an output amplifier coupled to the
3 directing circuit for providing an output signal independent of interface polarity
4 requirements.

1 16. The telecommunications interface system according to claim 15 wherein the
2 signal processing circuit further comprises an output automatic gain adjusting
3 circuit coupled to the output amplifier for providing an adjusted output signal
4 having a predetermined range of amplitudes.

1 17. The telecommunications interface system according to claim 16 wherein the
2 signal processing circuit further comprises means for manually controlling the gain
3 of the output signal, coupled between the output automatic gain adjusting circuit
4 and the means for controlling the directing circuit.

1 18. The telecommunications interface system according to claim 16 wherein the
2 circuit further comprises means for providing additional control of the output signal
3 coupled between the means for controlling the directing circuit and the output
4 amplifier.

1 19. The telecommunications interface system according to claim 16 wherein the
2 signal processing circuit further comprises means for amplifying the output signal,
3 coupled to the output automatic gain adjusting circuit.

1 20. The telecommunications interface system according to claim 19 wherein the
2 analog circuit further comprises means for reducing the level of noise on the output
3 signal coupled to the output voltage control amplifier.

1 21. The telecommunications interface system according to claim 20 wherein the
2 signal processing circuit further comprises an output reference low-pass filter
3 coupled to the means for sampling the input signal, for filtering the input reference
4 signal used to calibrate the output signal path in the directing circuit.

1 22. The telecommunications interface system according to claim 21 wherein the
2 signal processing circuit further comprises means for boosting the output signal

3 coupled to the output voltage control amplifier, to the means for reducing the level
4 of noise, and to the output reference low-pass filter, for boosting the output signal
5 level.

1 23. The telecommunications interface system according to claim 4 wherein the
2 signal processing circuit further comprises means for manually controlling the
3 means for controlling the directing circuit in order to provide the user with manual
4 control of the input and output signal gains.

1 24. The telecommunications interface system according to claim 6 wherein the
2 signal processing circuit further comprises means for placing the interface system in
3 a low power consumption state coupled to the input automatic gain adjusting
4 circuit, for conserving the interface system's power.

1 25. The telecommunications interface system according to claim 24 wherein the
2 signal processing circuit further comprises a bandgap reference circuit coupled to
3 the means for placing the interface system in a low power consumption state, to
4 provide a stable reference voltage that is applied to the decisional circuit.

1 26. The telecommunications interface system according to claim 1 wherein the
2 accessory is a voice accessory.

1 27. The telecommunications interface system according to claim 1 wherein the
2 accessory is a data accessory.

1 28. A CO Dialtone Learning Sequence method of learning the characteristics of
2 any telephone with a 4-wire port interface which comprises the steps of:

- 3 a. searching for a CO dialtone;
- 4 b. detecting a CO dialtone;
- 5 c. selecting receive lines;

- d. setting the receive channel sensitivity by comparison with receive level references;
- e. selecting transmit lines; and
- f. setting the transmit channel sensitivity by comparison with a transmit reference signal.

29. A Host Automated 800 Learning Sequence method of learning the characteristics of any telephone with a 4-wire port interface which comprises the steps of:

- a. searching for a DTMF tone by a host;
- b. sending a preamble to a user;
- c. disabling a reference signal;
- d. enabling a level detect system;
- e. measuring an incoming transmit signal;
- f. comparing the transmit signal against a transmit level reference;
- g. sending a level confirmation signal.

30. An SIT Automated 800 Learning Sequence method of learning the characteristics of any telephone with a 4-wire port interface which comprises the steps of:

- a. searching for a preamble;
- b. detecting the preamble;
- c. selecting receive lines;
- d. setting the receive lines' channel sensitivity by comparison with receive level references;
- e. selecting transmit lines; and
- f. setting the transmit lines' channel sensitivity by comparison with a transmit reference signal.

1 31. A Manual 800 method of learning the characteristics of any telephone with
2 a 4-wire port interface which comprises the steps of:

- 3 a. enabling a Manual 800 mode;
- 4 b. sending a preamble;
- 5 c. attenuating a transmit channel;
- 6 d. attenuating a receive channel;
- 7 e. enabling switching algorithms; and
- 8 f. disabling the Manual 800 mode.

1 32. A telecommunications interface system that automatically configures an
2 accessory having a predetermined number of electrical accessory contacts to
3 appropriately interface with a telephone base unit having two electrical output
4 contacts and two electrical input contacts, wherein the interface system is
5 configured for coupling the output contacts to a predetermined pair of the accessory
6 contacts and for also coupling the input contacts to a predetermined pair of
7 accessory contacts, the interface comprising:

- 8 a. an interface port having the predetermined number of accessory contacts,
9 wherein the port receives an input signal from the output contacts on two of
10 the accessory contacts;
- 11 b. an analog circuit having two signal inputs coupled for receiving the input
12 signal from the interface port and two signal outputs coupled for sending
13 the output signal from the signal processing circuit;
- 14 c. a crosspoint switch array coupled between the interface port and the analog
15 circuit for automatically electrically coupling the output contacts to the
16 signal inputs and the input contacts to the signal outputs; and
- 17 d. a controller coupled to the crosspoint switch array, for manipulating the
18 array in order to locate the appropriate input and output lines.

1 33. The telecommunications interface system according to claim 32 wherein the
2 analog circuit further comprises:

- a. a 32 bit addressable latch coupled to the crosspoint switch array for manipulating the coupling of the input and output contacts with the signal inputs and outputs, the 32 bit addressable latch further coupled to the shunt select array for fine tuning of the input and output signals;
- b. a receive input differential amplifier coupled to the crosspoint-switch array, for amplifying the difference between the two receive lines;
- c. a 1 KOhm resistor coupled between two receive lines of the input differential amplifier;
- d. a receive input step attenuator coupled to the differential amplifier for providing an adjusted input signal regardless of impedance and sensitivity characteristics of the telephone base unit;
- e. an input multiplexer coupled between the input step attenuator and the 32 bit addressable latch, for providing manual control of the input signal sensitivity;
- f. an input voltage control amplifier coupled to the input step attenuator for providing volume control of the input signal;
- g. an automatic level control circuit coupled between the input voltage control amplifier and the controller, for providing a dynamic output limiting system to protect a user from prolonged high decibel sounds;
- h. an output amplifier coupled to the input voltage control amplifier for driving an inductive load;
- i. a switchable dialtone filter coupled between the input step attenuator and the 32 bit addressable latch to provide a means for decisionally filtering certain signals;
- j. an anti-alias filter coupled to the switchable dialtone filter;
- k. a sample and hold circuit coupled between the anti-alias filter and the controller for sampling the input signal in order to determine when the appropriate input and output lines are located;

- 31 l. a sampling circuit coupled to the clock pins of the switchable dialtone filter,
32 the anti-alias and the sample and hold circuit, for sampling a fraction of the
33 input signal;
- 34 m. an output differential amplifier coupled to the crosspoint switch array
35 for providing an output signal;
- 36 n. an output step attenuator having a predetermined range of values, coupled to
37 the output differential amplifier for automatically adjusting the gain of the
38 output signal;
- 39 o. an output multiplexer coupled between the output step attenuator and the 32
40 bit addressable latch for manually controlling the output step attenuator;
- 41 p. a shunt select circuit coupled in parallel with the interface port and the
42 crosspoint switch array to provide additional control of the output signal;
- 43 q. an output voltage control amplifier coupled to the output step attenuator, for
44 amplifying the output signal;
- 45 r. an expander circuit coupled to the output voltage control amplifier for
46 reducing noise in the output signal by utilizing electronic noise reduction;
- 47 s. an output reference low-pass filter coupled to the anti-alias filter, for
48 filtering the input reference signal used to calibrate the output signal path in
49 the crosspoint switch array;
- 50 t. an output preamplifier coupled to the output voltage control amplifier, the
51 expander circuit and the output reference low-pass filter, for boosting the
52 output signal level before it reaches the voltage control amplifier;
- 53 u. a mode latch coupled to the 32 bit addressable latch which allows the user
54 to manually control the input and output step attenuators;
- 55 v. a sleep and system power supply circuit coupled to the input step attenuator
56 which monitors the input signal and places the analog circuit in a standby
57 mode when the receive signal falls below a threshold level in order to
58 conserve power, and also couples with a power source;

59 w. a bandgap filter coupled between the sleep and system power supply
60 circuit and the controller for providing a stable reference signal to the
61 controller.

1 34. The telecommunications system according to claim 33 wherein the load is
2 inductive.

1 35. The telecommunications system according to claim 34 wherein the inductive
2 load is a headset.

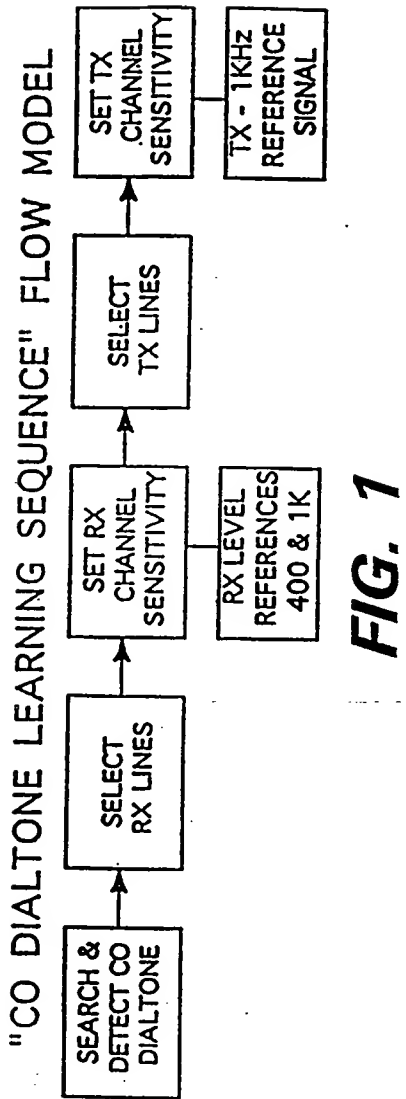
1 36. The telecommunications system according to claim 34 wherein the inductive
2 load is a handset.

1 37. The telecommunications system according to claim 33 wherein the load is
2 capacitive.

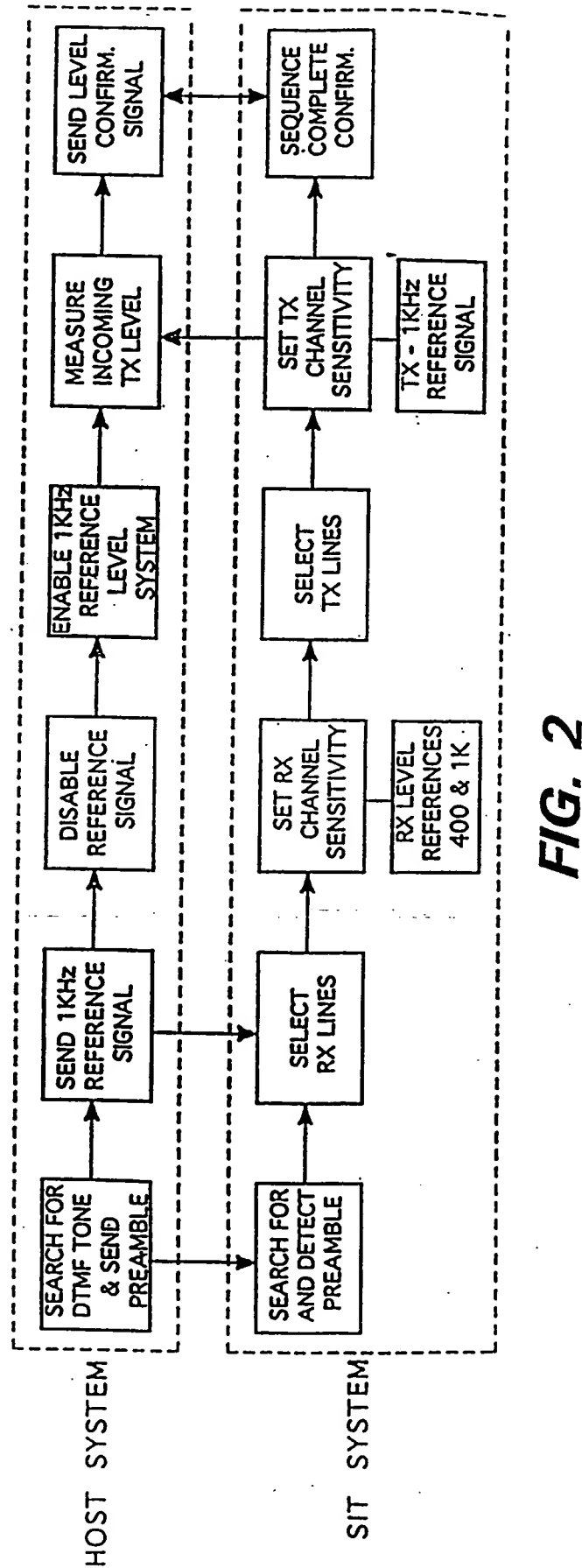
1 38. The telecommunications system according to claim 33 wherein the load is
2 resistive.

1 39. The telecommunications system according to claim 33 wherein the
2 accessory is a voice accessory.

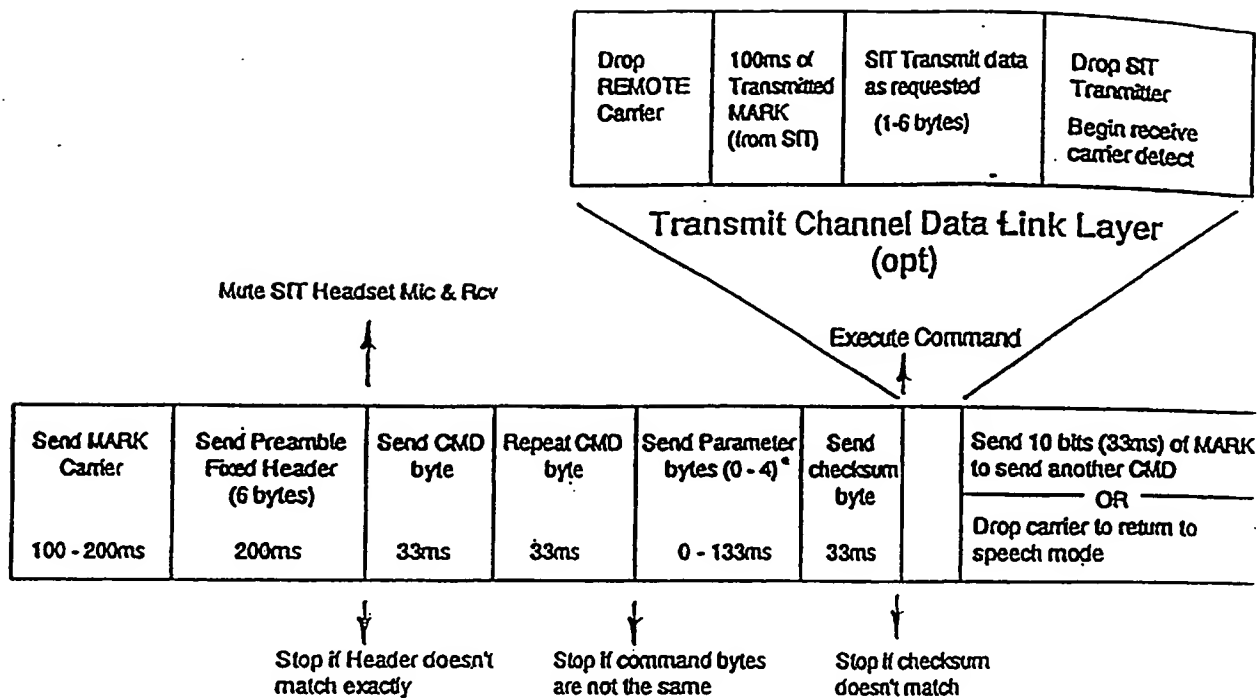
1 40. The telecommunications system according to claim 33 wherein the
2 accessory is a data accessory.



"AUTOMATED 800 LEARNING SEQUENCE" FLOW MODEL

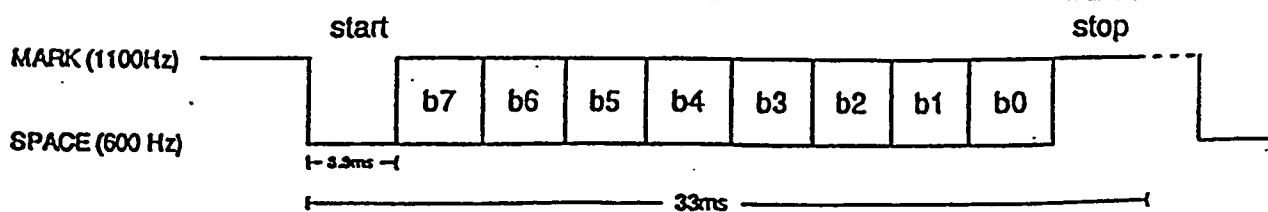


2 / 8



NOTE: The number of parameters is directly dependent on the Command type

Receive Channel Data Link Layer

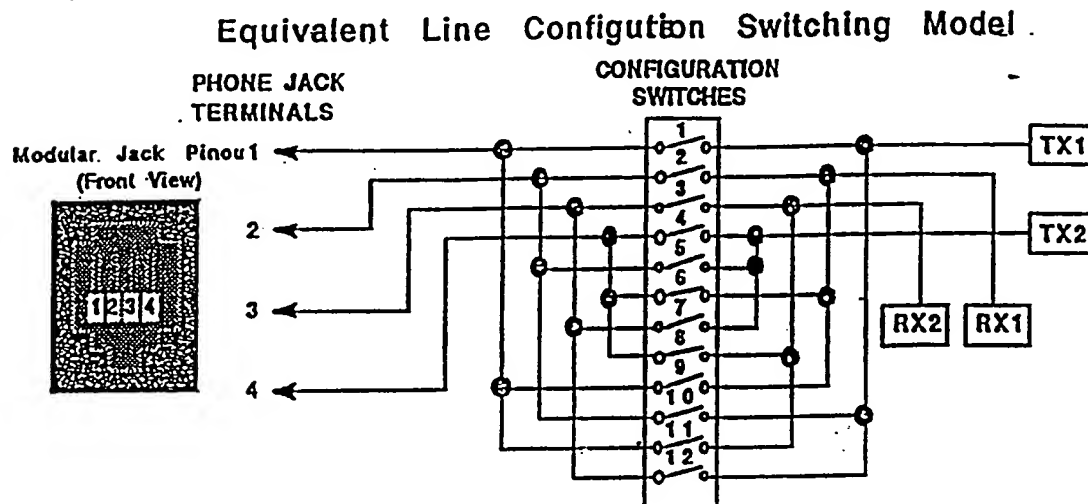


Receive Channel Physical Layer

FIG. 3

Smart Interface Technology (SIT) Project

Preliminary Line Configuration Switching Algorithms and Model



<u>Dialtone Detection</u>	<u>Rx Pinout</u>	<u>Tx Pinout Sequence'</u>	<u>Algorithm Ref. No.</u>	<u>Model Sw. "ON"</u>
Pins 2 & 3	Pins 2 & 3	Pins 1 & 4 (Primary)	1	1,2,3,4
Pins 2 & 3	Pins 2 & 3	Pins 1 & 2 (2nd Try)	2	1,2,3,5
Pins 2 & 3	Pins 2 & 3	Pins 1 & 3 (3rd Try)	3	1,2,3,7
Pins 2 & 3	Pins 2 & 3	Pins 4 & 2 (4th Try)	4	2,3,4,10
Pins 2 & 3	Pins 2 & 3	Pins 4 & 3 (5th Try)	5	2,3,4,12
Pins 2 & 4	Pins 2 & 4	Pins 1 & 3 (Primary)	6	1,2,7,8
Pins 2 & 4	Pins 2 & 4	Pins 1 & 2 (2nd Try)	7	1,2,5,8
Pins 2 & 4	Pins 2 & 4	Pins 1 & 4 (3rd Try)	8	1,2,4,8
Pins 2 & 4	Pins 2 & 4	Pins 3 & 2 (4th Try)	9	2,5,8,12
Pins 2 & 4	Pins 2 & 4	Pins 3 & 4 (5th Try)	10	2,4,8,12
Pins 1 & 2	Pins 1 & 2	Pins 3 & 4 (Primary)	11	2,4,11,12
Pins 1 & 2	Pins 1 & 2	Pins 3 & 1 (2nd Try)	12	1,2,11,12
Pins 1 & 2	Pins 1 & 2	Pins 3 & 2 (3rd Try)	13	2,5,11,12
Pins 1 & 2	Pins 1 & 2	Pins 4 & 1 (4th Try)	14	1,2,4,11
Pins 1 & 2	Pins 1 & 2	Pins 4 & 2 (5th Try)	15	2,4,10,11
Pins 1 & 3	Pins 1 & 3	Pins 2 & 4 (Primary)	16	3,4,9,11
Pins 1 & 3	Pins 1 & 3	Pins 2 & 1 (2nd Try)	17	1,3,5,9
Pins 1 & 3	Pins 1 & 3	Pins 2 & 3 (3rd Try)	18	3,5,9,12
Pins 1 & 3	Pins 1 & 3	Pins 4 & 1 (4th Try)	19	1,3,4,9
Pins 1 & 3	Pins 1 & 3	Pins 4 & 3 (5th Try)	20	3,4,9,12

FIG. 4

<u>Dialtone Detection</u>	<u>Rx Pinout</u>	<u>Tx-Pinout Sequence</u>	<u>Algorithm Ref. No.</u>	<u>Model Sw. "ON"</u>
Pins 1 & 4	Pins 1 & 4	Pins 2 & 3 (Primary)	21	7,8,9,10
Pins 1 & 4	Pins 1 & 4	Pins 2 & 1 (2nd Try)	22	1,5,8,9
Pins 1 & 4	Pins 1 & 4	Pins 2 & 4 (3rd Try)	23	4,8,9,10
Pins 1 & 4	Pins 1 & 4	Pins 3 & 1 (4th Try)	24	1,7,8,9
Pins 1 & 4	Pins 1 & 4	Pins 3 & 4 (5th Try)	25	4,8,9,12
Pins 3 & 4	Pins 3 & 4	Pins 1 & 2 (Primary)	26	1,3,5,6
Pins 3 & 4	Pins 3 & 4	Pins 1 & 3 (2nd Try)	27	1,3,6,7
Pins 3 & 4	Pins 3 & 4	Pins 1 & 4 (3rd Try)	28	1,3,4,6
Pins 3 & 4	Pins 3 & 4	Pins 2 & 3 (4th Try)	29	3,6,7,10
Pins 3 & 4	Pins 3 & 4	Pins 2 & 4 (5th Try)	30	3,4,6,10

<u>ALGORITHM REF. NUMBER</u>	<u>SWITCHING MODEL ACTION</u>	<u>ALGORITHM REF. NUMBER</u>	<u>SWITCHING MODEL ACTION</u>
31	Switch 1: "ON"	43	Switch 7: "ON"
32	Switch 1: "OFF"	44	Switch 7: "OFF"
33	Switch 2: "ON"	45	Switch 8: "ON"
34	Switch 2: "OFF"	46	Switch 8: "OFF"
35	Switch 3: "ON"	47	Switch 9: "ON"
36	Switch 3: "OFF"	48	Switch 9: "OFF"
37	Switch 4: "ON"	49	Switch 10: "ON"
38	Switch 4: "OFF"	50	Switch 10: "OFF"
39	Switch 5: "ON"	51	Switch 11: "ON"
40	Switch 5: "OFF"	52	Switch 11: "OFF"
41	Switch 6: "ON"	53	Switch 12: "ON"
42	Switch 6: "OFF"	54	Switch 12: "OFF"

NOTES:

- 1) Algorithm No. 1 will be the default setting for system power-up, hard or soft resets and "learning" timeout conditions.
- 2) Ideally all 12 equivalent switches can be selected and switched "on" or "off" independant of the above algorithm's.

FIG. 5

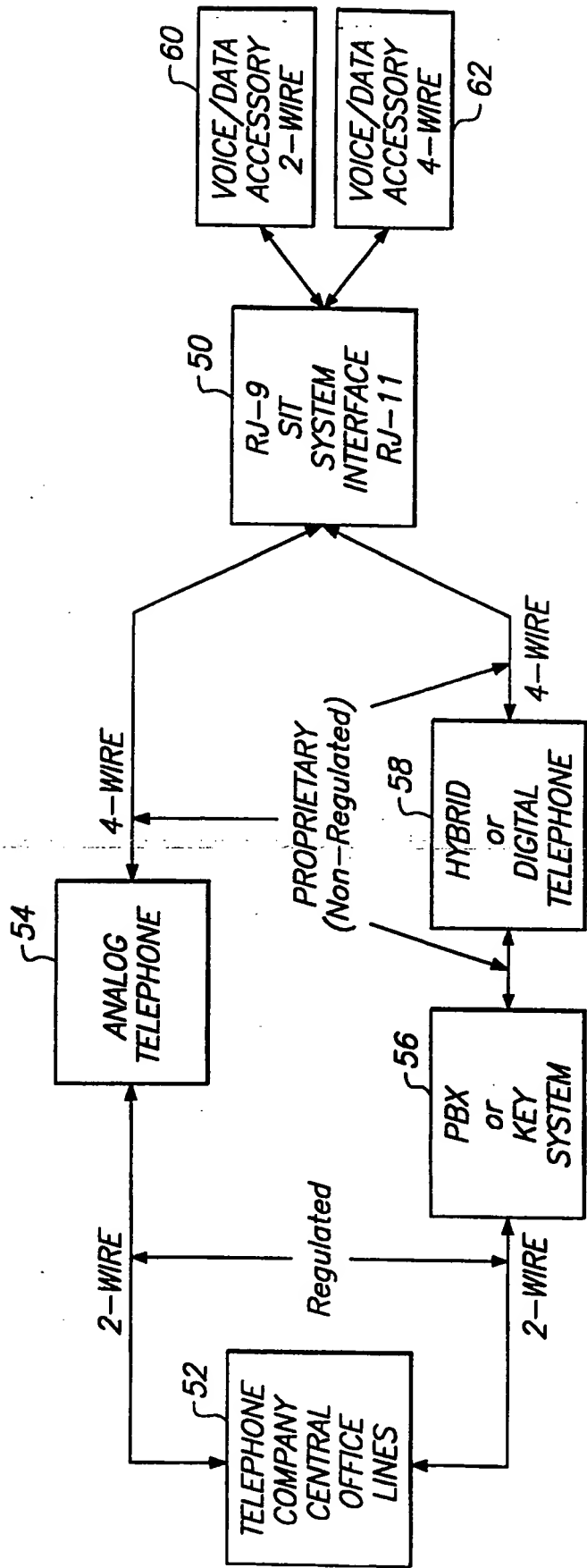


FIG. 6

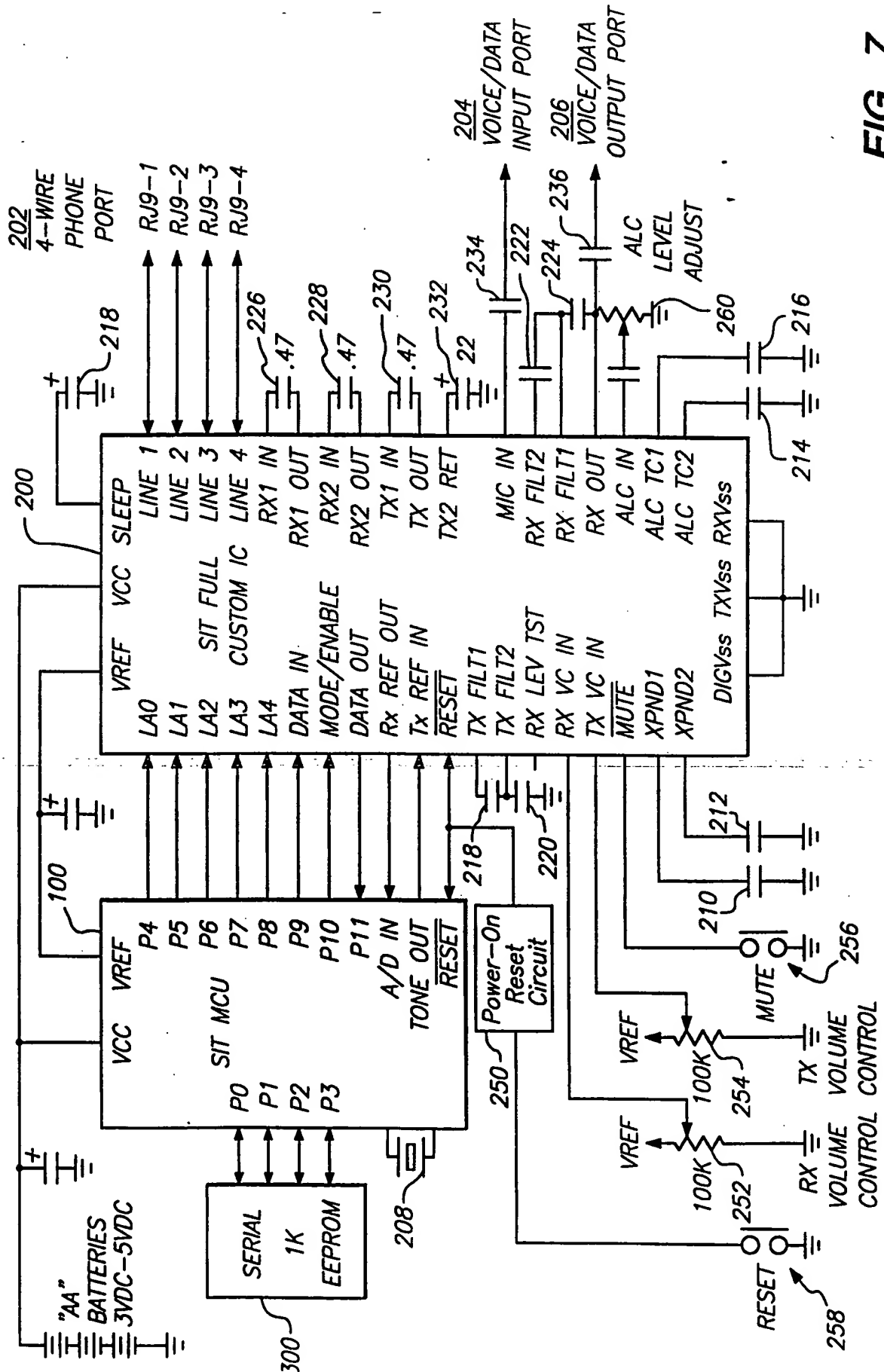


FIG. 7

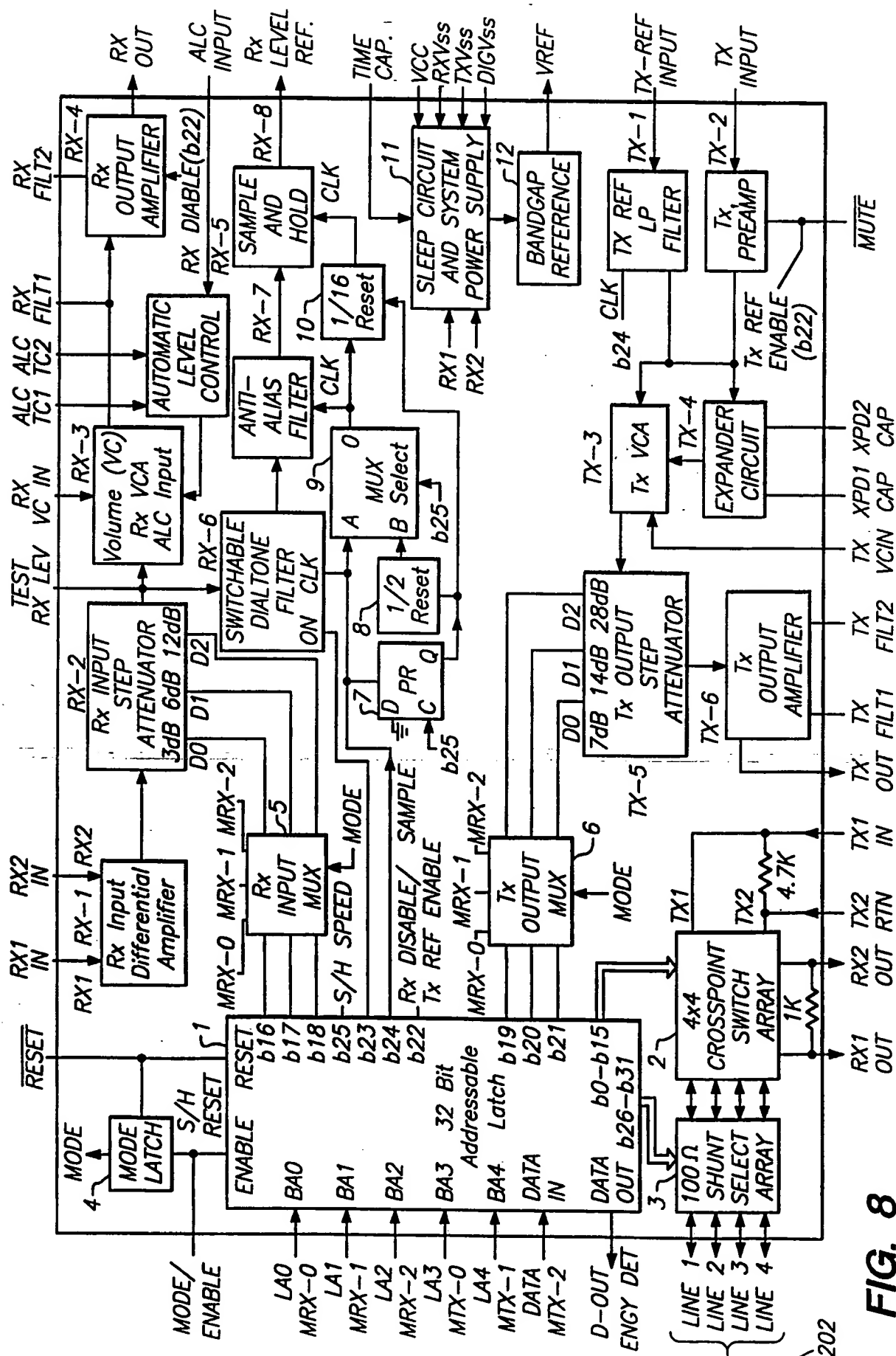
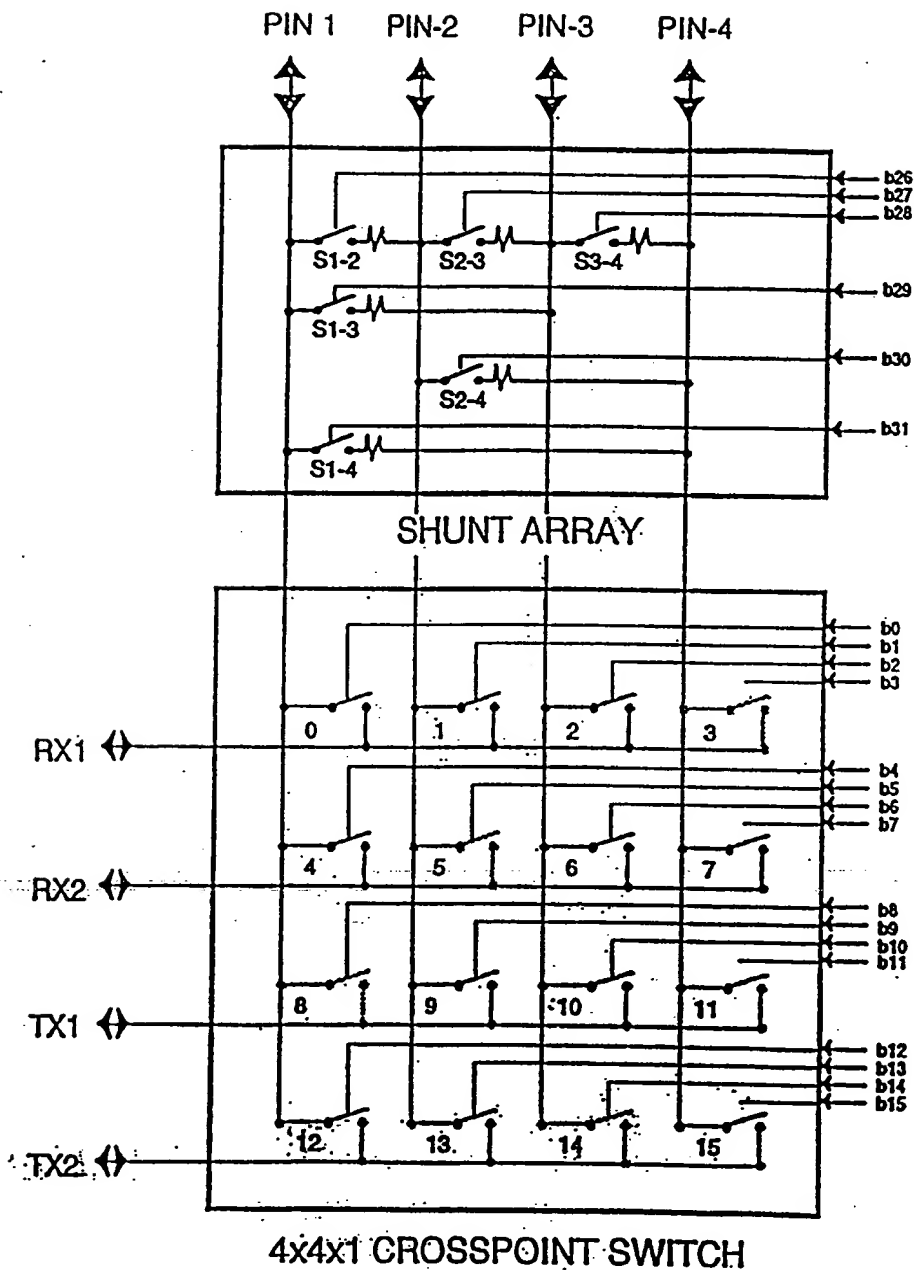


FIG. 8

8 / 8

**FIG. 9**